REMARKS

Claims 47-49, 51-54 and 57-58 are pending. Claims 47, 51, 51, 57 and 58 were amended to address the Examiner's rejections under 35 U.S.C. § 112, second paragraph. The remarks below address the rejections in the Final Office Action dated October 24, 2005.

New claim limitations

No new matter was added in the current claim amendments. The new claim limitations are clearly supported by at least paragraph [046] that spans pages 19-20 of the present specification.

35 U.S.C. § 112 second paragraph rejections

Claims 47 and 51 were amended to recite how the various claim elements can be operated overlapped in time, and to provide a relationship between the interleaver apparatus recited in the preamble and the subsequent claim limitations.

Claims 57 and 58 were amended to address the antecedent basis issue raised by the Examiner.

Withdrawal of this rejection as it pertains to the amended claims is respectfully requested.

35 U.S.C. § 101 rejection

Claims 47-49, 51-54, 57 and 58 were rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. This rejection is traversed.

In the Final Rejection, the Examiner asserts that the claims recite an abstract mathematical algorithm that can be carried out by hand and is therefore non-statutory. This is incorrect. Claim 47 explicitly recites an "apparatus for interleaving" having at least four specific elements that perform the interleaving, as well as algorithms for manipulating data using the structure. Claim 51 recites a "method for interleaving" that includes four steps that use specific structure to carry out the steps. That is, to perform the claimed interleaving, there must be

structural elements to manipulate data and an algorithm to control how the data is manipulated. FIG. 2A and FIG. 7 show exemplary structure to perform the interleaving, and FIGS. 8 and 9 show exemplary interleaver algorithms.

MPEP 2106, section IV, (b)(1) provides the following general guidelines in determining if a claim recites non-statutory subject matter:

> If the "acts" of a claimed process manipulate only numbers, abstract concepts or ideas, or signals representing any of the foregoing, the acts are not being applied to appropriate subject matter. *Schrader*, 22 F.3d at 294-95, 30 USPQ2d at 1458-59. Thus, a process consisting solely of mathematical operations, i.e., converting one set of numbers into another set of numbers, does not manipulate appropriate subject matter and thus cannot constitute a statutory process.
>
> In practical terms, claims define nonstatutory processes if they:
> - consist solely of mathematical operations without some claimed practical application (i.e., executing a "mathematical algorithm"); or
>
> - simply manipulate abstract ideas, e.g., a bid (*Schrader*, 22 F.3d at 293-94, 30 USPQ2d at 1458-59) or a bubble hierarchy (*Warmerdam*, 33 F.3d at 1360, 31 USPQ2d at 1759), without some claimed practical application.

Interleavers are devices that process and reorder data. The data can be any real-world data, such as data that was transmitted and is captured at a receiver. The data is never merely "numbers, abstract concepts or ideas, or signals representing any of the foregoing." There is always a practical application to using an interleaver, specifically, to process and reorder real data.

In this manner, interleavers are similar to A/D converters. Both are structural devices that accept any form of real-world data and transform the data. Both employ algorithms to transform the data. Interleavers and A/D converters are both patentable subject matter. The mere fact that algorithms are used does not render such devices as being non-statutory, whether claimed in apparatus or method form.

Furthermore, even an interleaver algorithm, taken alone (i.e., without any implementing structure) constitutes statutory subject matter. MPEP 2106, section IV, (b)(1) provides the following general guidelines in determining if a mathematical algorithm recites non-statutory subject matter:

> Certain mathematical algorithms have been held to be nonstatutory because they represent a mathematical definition of a law of nature or a natural phenomenon. For example, a mathematical algorithm representing the formula $E = mc^2$ is a "law of nature" - it defines a "fundamental scientific truth" (i.e., the relationship between energy and mass). To comprehend how the law of nature relates to any object, one invariably has to perform certain steps (e.g., multiplying a number representing the mass of an object by the square of a number representing the speed of light). In such a case, a claimed process which consists solely of the steps that one must follow to solve the mathematical representation of $E = mc^2$ is indistinguishable from the law of nature and would "preempt" the law of nature. A patent cannot be granted on such a process.

An interleaver algorithm is not a law of nature or a natural phenomenon. It is a man-made creation. Thus, the claimed invention is further considered to be statutory because it recites an interleaver algorithm within the claim language. That is, the combination of statutory structure that implements a statutory algorithm (claim 47) and a statutory algorithm that is implemented via statutory structure (claim 51) are both statutory inventions under 35 U.S.C. § 101.

If the Examiner rejects the claims again under § 101, it is requested that a detailed explanation be provided regarding why the claims do not conform with the guidelines for statutory subject matter as set forth in MPEP 2106, section IV, (b)(1), as well as how the claimed interleaver and method of interleaving differ from the innumerable interleavers and interleaver methods that are routinely patented every year (see the attached Appendix of interleaver patents).

For at least the reasons set forth above, withdrawal of the § 101 rejection is respectfully requested.

Prior Art Rejections

Claims 47-49, 51-54, 57 and 58 were rejected under 35 U.S.C. § 103(a) as being unpatentable over 3GPP document (3rd Generation Partnership Project; Technical Specification Group; Group Radio Access Network; Multiplexing and channel coding (FDD); (3G TS 25.212 version 3.1.0) (1999)) in view of U.S. Patent No. 6,845,482 (Yao, et al.).

1. Patentability of independent claims 47 and 51 over the 3GPP document in view of Yao

On page 8 of the Final Rejection, the Examiner admits that the 3GPP document does not explicitly teach simultaneous intra-block and inter-block permutations. The Examiner now relies upon Yao for a disclosure of the claim limitations directed to simultaneous intra-block and inter-block permutations. However, as discussed below, Yao also does not disclose or suggest such any such limitations, and thus does not make up for the deficiencies in the 3GPP document.

In the Final Rejection, the Examiner states that Fig. 6B of Yao teaches inter-row permutations, in which an inter-row permutation inherently permutes individual elements of each column, hence is also an intra-column permutation. The Examiner further asserts that an inter-row permutation is an inter-block permutation and intra-column permutation is an intra-block permutation, which are the same or equivalent to the simultaneous inter-block and intra-block permutations of the present invention. This is incorrect. Figs. 6A-6B of Yao disclose a method for performing intra-block and inter-block permutations and are described in column 9, line 59 through column 14, line 43. Referring to this text portion, the method disclosed by Yao is a simplified method of the 3GPP standard. For example, stage 1 must be completed first before stage 2 can perform an intra-row permutation. Then stage 3 performs an inter-row permutation after stages 1 and 2, which is sequential and not simultaneously with either stages 1 and 2.

Figs. 6A-6B of Yao discloses that a first stage is completed for an order in which bits in a code segment are written (i.e., stored) to an array of size RxC. Referring again to the text of column 9, line 59 through column 14, line 43, during a first stage, an array is filled one row at a time and if the code sequence is not equal to the size of the array, then empty cells occur in the array. A second stage is then performed where the elements of each row are permuted on the stored array. A third stage is then performed for permuting the rows in the stored array. After the inter-row permutation of the third stage, the bits are then read out column-by-column from the stored RxC array. Thus, Yao teaches away from simultaneous inter-block and intra-block permutations because the bits can only be read out of the stored array after stage 3 is performed.

For example, in order to achieve an interleaving for a practical implementation, the bits for a code segment are first stored to a memory unit in a particular order (e.g., interleaved or linear), which then are retrieved from the memory unit in a complementary order (e.g., interleaved or linear). See column 12, line 59 through column 13, line 9, which reads as follows:

> As shown above, the interleaving defined by W-CDMA standard is a complicated process. In a practical implementation, to achieve the interleaving, the bits for a code segment are stored to a memory unit in a particular order (e.g., either linear or interleaved) and are retrieved from the memory unit in the complementary order (i.e., interleaved or linear).
>
> Aspects of the invention provide techniques to efficiently generate memory addresses needed to perform interleaving for the Turbo code defined by the W-CDMA standard. In an aspect, to expedite address generation, a number of look-up tables (LUTs) are provided to store various sequences of values used to generate interleaved addresses. The use of these tables expedites the address computations and allows the required addresses to be generated in less time. The address generation may thus not be the bottleneck for the Turbo decoding. Some of these tables and the sequences stored therein are described below.

In sum, Yao teaches away from simultaneous intra-block and inter-block permutations since it is a simplified method of the 3GPP standard.

2. Patentability of dependent claims

The dependent claims are believed to be patentable over the applied references for at least the reason that they are dependent upon allowable base claims and because they recite additional patentable elements and steps.

Conclusion

Insofar as the Examiner's rejections were fully addressed, the instant application is in condition for allowance. A Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,

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Enclosure: Appendix (4 pages)

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APPENDIX

(attachment to "Reply Accompanying RCE Request" for Application No. 10/066,658)

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Searching 1976 to present...

Results of Search in 1976 to present db for:
TTL/interleaver AND ACLM/interleaver: 87 patents.
Hits 1 through 50 out of 87

Final 37 Hits

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Refine Search TTL/interleaver AND ACLM/interleaver

	PAT. NO.		Title
1	6,988,234	T	Apparatus and method for memory sharing between interleaver and deinterleaver in a turbo decoder
2	6,987,752	T	Method and apparatus for frequency offset estimation and interleaver synchronization using periodic signature sequences
3	6,965,557	T	Interleaver memory access apparatus and method of CDMA system
4	6,965,479	T	Optical filter, interleaver, and optical communication system
5	6,954,832	T	Interleaver for iterative decoder
6	6,947,491	T	Third generation FDD modem interleaver
7	6,925,587	T	Turbo code interleaver with near optimal performance
8	6,917,760	T	Wide passband optical interleaver
9	6,909,531	T	Optical (de-)interleaver and method of (de-)interleaving optical signals
10	6,903,665	T	Method and apparatus for error control coding in communication systems using an outer interleaver
11	6,900,938	T	Low dispersion interleaver
12	6,892,342	T	Sets of rate-compatible universal turbo codes nearly optimized over various rates and interleaver sizes
13	6,871,303	T	Random-access multi-directional CDMA2000 turbo code interleaver
14	6,862,707	T	Turbo code encoder having an improved interleaver
15	6,857,087	T	High-performance low-memory interleaver banks for turbo-codes
16	6,845,482	T	Interleaver for turbo decoder
17	6,823,002	T	Linear block interleaver for discrete multi-tone modulation

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18 6,798,551 T Gires-Tournois interferometer with faraday rotators for optical signal interleaver
19 6,791,753 T Retro-reflective fiber optic interleaver
20 6,785,862 T Convolutional interleaver employing an efficient memory scheme
21 6,785,859 T Interleaver for variable block size
22 6,782,157 T Bidirectional optical interleaver
23 6,781,754 T Interleaver using spatial birefringent elements
24 6,775,435 T Wavelength interleaver
25 6,772,391 T Hybrid interleaver for turbo codes
26 6,768,843 T Cascaded fourier filter interleaver having enhanced performance
27 6,768,591 T Interleaver
28 6,741,813 T Interference-based DWDM optical interleaver using beam splitting and selective phase shifting and re-combining
29 6,735,365 T Fused fiber interleaver
30 6,732,316 T Data interleaver and method of interleaving data
31 6,724,539 T Interleaver
32 6,718,503 T Reduced latency interleaver utilizing shortened first codeword
33 6,715,124 T Trellis interleaver and feedback precoder
34 6,701,467 T Interleaver device and method for interleaving a data set
35 6,697,990 T Interleaver design for parsed parallel concatenated codes
36 6,691,261 T De-interleaver and method of de-interleaving
37 6,690,513 T Rhomb interleaver
38 6,684,361 T Data interleaver and method of interleaving data
39 6,680,470 T Interleaver with thermal and chromatic dispersion compensation
40 6,661,771 T Method and apparatus for interleaver synchronization in an orthogonal frequency division multiplexing (OFDM) communication system
41 6,658,181 T Polarization interleaver
42 6,658,172 T Optical system with 1.times.N interleaver and methods of making and using same
43 6,654,514 T Tuned fiber optic interleaver
44 6,643,064 T Optical signal interleaver
45 6,643,063 T Deinterleaver with high isolation and dispersion compensation and 50/200GHz interleaver and deinterleaver
46 6,639,707 T Tandem interleaver
47 6,637,000 T Turbo code interleaver using linear congruential sequences
48 6,634,009 T Interleaver-deinterleaver megacore
49 6,625,763 T Block interleaver and de-interleaver with buffer to reduce power consumption
50 6,625,113 T Digital signal frame and interleaver synchronizer

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TTL/interleaver AND ACLM/interleaver: 87 patents.
*Hits **51** through **87** out of **87***

Prev. 50 Hits

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Refine Search TTL/interleaver AND ACLM/interleaver

	PAT. NO.		Title
51	6,624,939	T	50/100 and 50/200 GHz de-interleaver with high isolation and dispersion compensation
52	6,597,842	T	Optical interleaver with image transfer element
53	6,591,038	T	Optical interleaver and demultiplexing apparatus for wavelength division multiplexed optical communications
54	6,574,049	T	Optical interleaver and de-interleaver
55	6,563,641	T	Fold interleaver
56	6,560,380	T	Planar lightwave circuit interleaver
57	6,516,437	T	Turbo decoder control for use with a programmable interleaver, variable block length, and multiple code rates
58	6,453,442	T	Two stage S--Random interleaver
59	6,449,277	T	Interleaver for parallel 8 bit cell of ATM systems and a method therefor
60	6,441,961	T	Folded optical interleaver with optional routing capability
61	6,411,654	T	Convolutional interleaver, convolutional deinterleaver, convolutional interleaving method, and convolutional deinterleaving method
62	6,400,508	T	Compact wavelength interleaver
63	6,370,669	T	Sets of rate-compatible universal turbo codes nearly optimized over various rates and interleaver sizes
64	6,366,390	T	Pulse interleaver
65	6,356,528	T	Interleaver and deinterleaver for use in a diversity transmission communication system
66	6,351,832	T	Turbo code symbol interleaver
67	6,334,197	T	Turbo code interleaver with near optimal performance

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68 6,304,991 T Turbo code interleaver using linear congruential sequence
69 6,222,958 T Optical interleaver/de-interleaver
70 6,215,923 T Optical interleaver
71 6,212,313 T Optical interleaver
72 6,178,530 T Addressing scheme for convolutional interleaver/de-interleaver
73 6,169,626 T Optical signal interleaver
74 6,064,664 T Base-band interleaver for code division multiple access mobile telecommunication system
75 6,035,427 T Convolutional interleaver and method for generating memory address therefor
76 5,948,357 T Heat resistant paper interleaver for sheet metal
77 5,933,431 T Frame-based modulus interleaver
78 5,898,698 T Multiple codeword interleaver method and apparatus
79 5,771,239 T Method and apparatus for modifying a transport packet stream to provide concatenated synchronization bytes at interleaver output
80 5,761,249 T Synchronization arrangement for decoder/de-interleaver
81 5,659,580 T Data interleaver for use with mobile communication systems and having a contiguous counter and an address twister
82 5,563,887 T Transmission error correction code appending device which can regulate a maximum delay of an interleaver in a variable bit rate video coding system
83 5,537,420 T Convolutional interleaver with reduced memory requirements and address generator therefor
84 5,519,734 T Synchronization arrangement for decoder-de-interleaver
85 5,483,541 T Permuted interleaver
86 4,768,325 T Paper interleaver for food patty molding machine
87 4,253,651 T Document interleaver device

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